

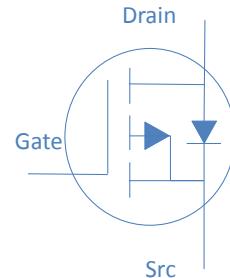
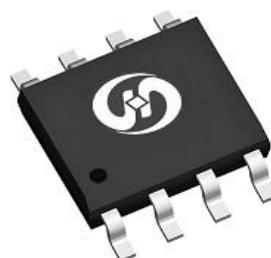
30V P-Ch Power MOSFET
Feature

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

V_{DS}	-30	V
$R_{DS(on),typ}$	$V_{GS}=10V$	17.5 mΩ
$R_{DS(on),typ}$	$V_{GS}=4.5V$	26 mΩ
I_D (Silicon Limited)	-10	A

Application

- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

SOIC-8


Part Number	Package	Marking
HTS200P03	SOIC-8	TS200P03

Absolute Maximum Ratings at $T_j=25^\circ C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25^\circ C$	-10	A
		$T_C=100^\circ C$	-8	
Drain to Source Voltage	V_{DS}	-	-30	V
Gate to Source Voltage	V_{GS}	-	± 25	V
Pulsed Drain Current	I_{DM}	-	-40	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.1mH, T_C=25^\circ C$	5.00	mJ
Power Dissipation	P_D	$T_A=25^\circ C$	2.5	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	°C

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	°C/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	°C/W

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=-250\mu\text{A}$	-30	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_D=-250\mu\text{A}$	-1.0	-1.5	-3.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-24\text{V}, T_j=25^\circ\text{C}$	-	-	-1	μA
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-20\text{V}, T_j=125^\circ\text{C}$	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
		$V_{\text{GS}}=\pm 25\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 500	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=-10\text{V}, I_D=-10\text{A}$	-	17.5	20	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_D=-7\text{A}$	-	26	35	
Transconductance	g_{fs}	$V_{\text{DS}}=-5\text{V}, I_D=-10\text{A}$	-	24	-	S
Gate Resistance	R_G	$V_{\text{GS}}=15\text{mV}, V_{\text{DS}}=0\text{V}, f=1\text{MHz}$	-	4.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-15\text{V}, f=1\text{MHz}$	-	1407	-	pF
Output Capacitance	C_{oss}		-	208	-	
Reverse Transfer Capacitance	C_{rss}		-	164	-	
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{DD}}=-15\text{V}, I_D=-13\text{A}, V_{\text{GS}}=-10\text{V}$	-	20.3	-	nC
	$Q_g(4.5\text{V})$		-	9.8	-	
Gate to Source Charge	Q_{gs}		-	3.2	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4.9	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=-15\text{V}, I_D=-1\text{A}, V_{\text{GS}}=-10\text{V}, R_G=2.7\Omega$	-	10	-	ns
Rise time	t_r		-	8	-	
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	25	-	
Fall Time	t_f		-	6	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_F=-3\text{A}$	-		-1.2	V
Reverse Recovery Time	t_{rr}	$I_F=-3\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$	-	32	-	ns
Reverse Recovery Charge	Q_{rr}		-	26	-	nC

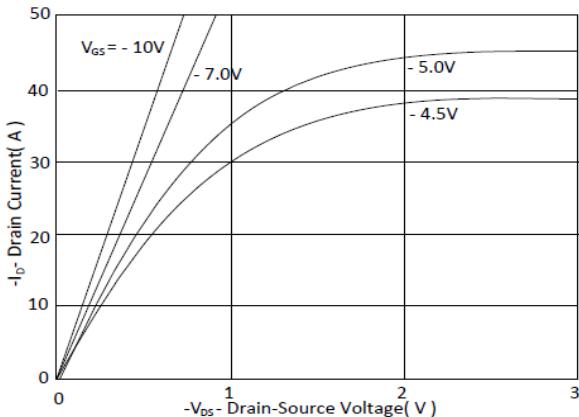
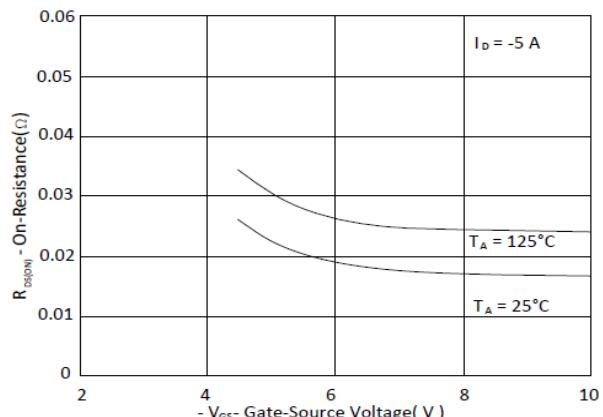
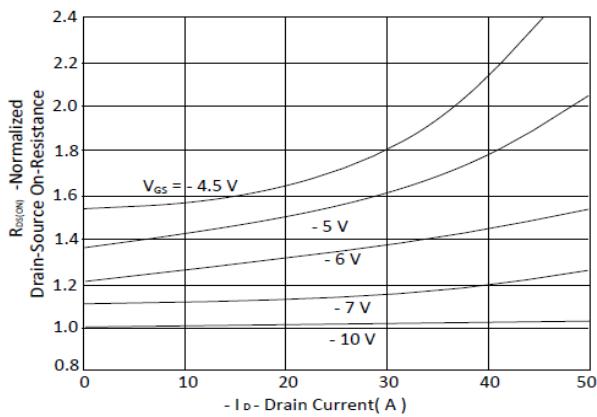
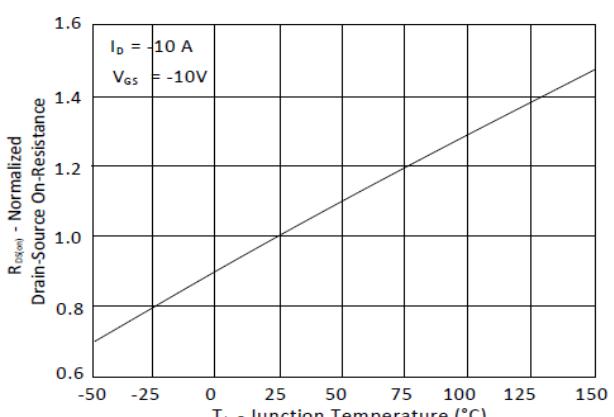
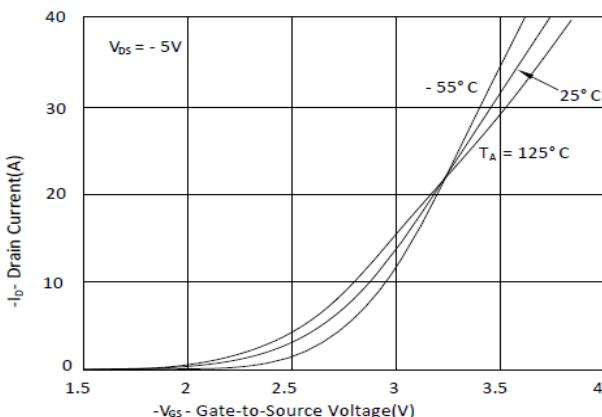
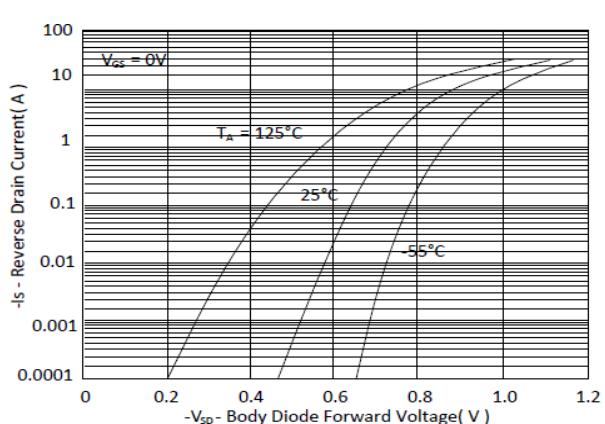
Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Transfer Characteristics

Figure 6. Typical Source-Drain Diode Forward Voltage


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

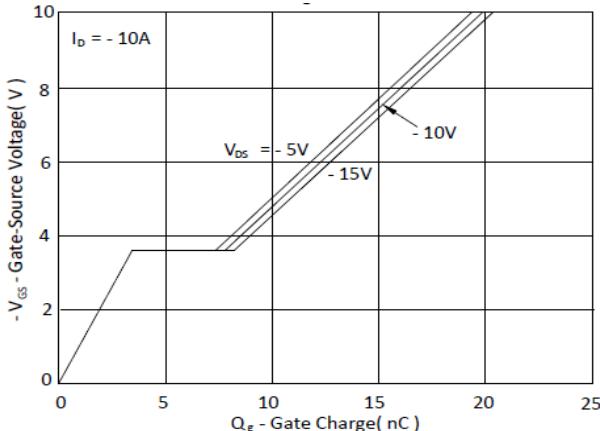


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

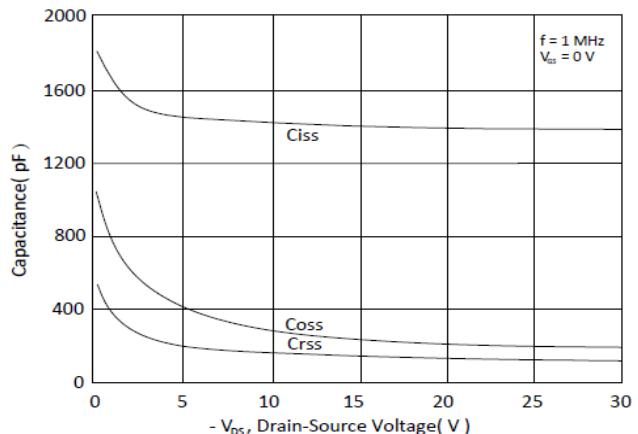


Figure 9. Maximum Safe Operating Area

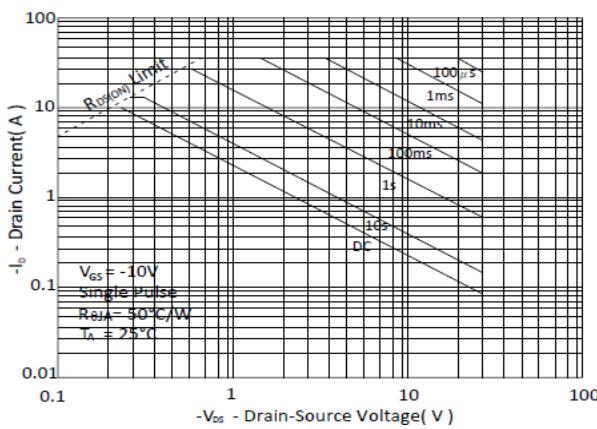


Figure 10. Single Pulse Maximum Power Dissipation

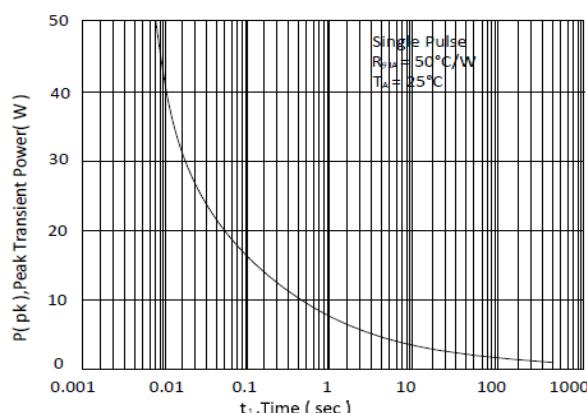
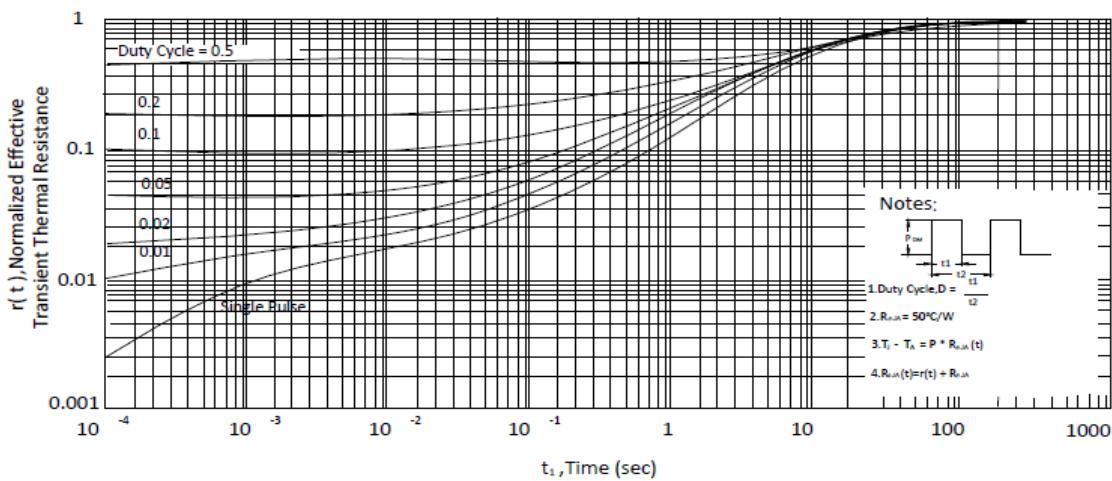
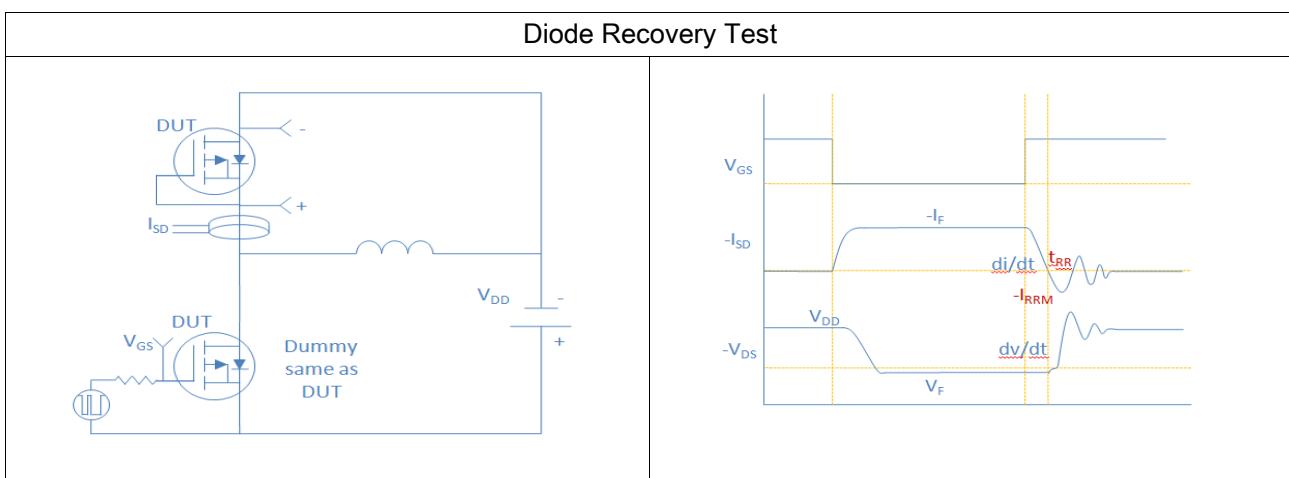
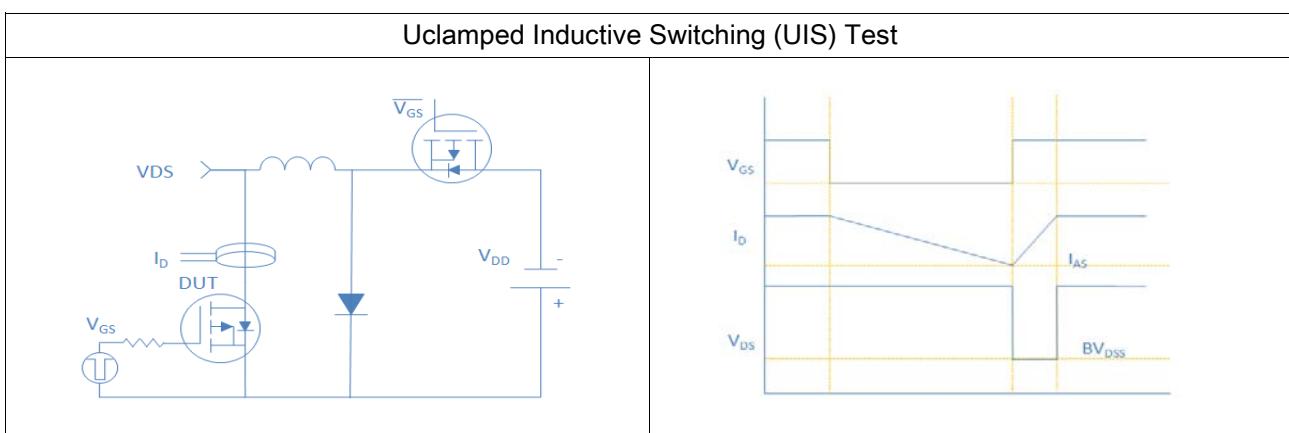
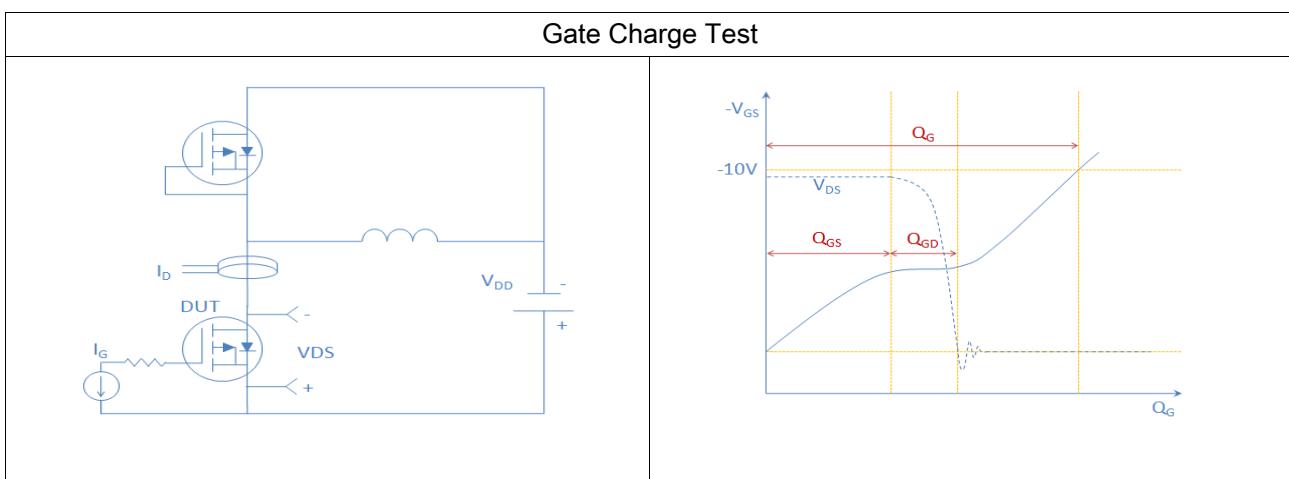
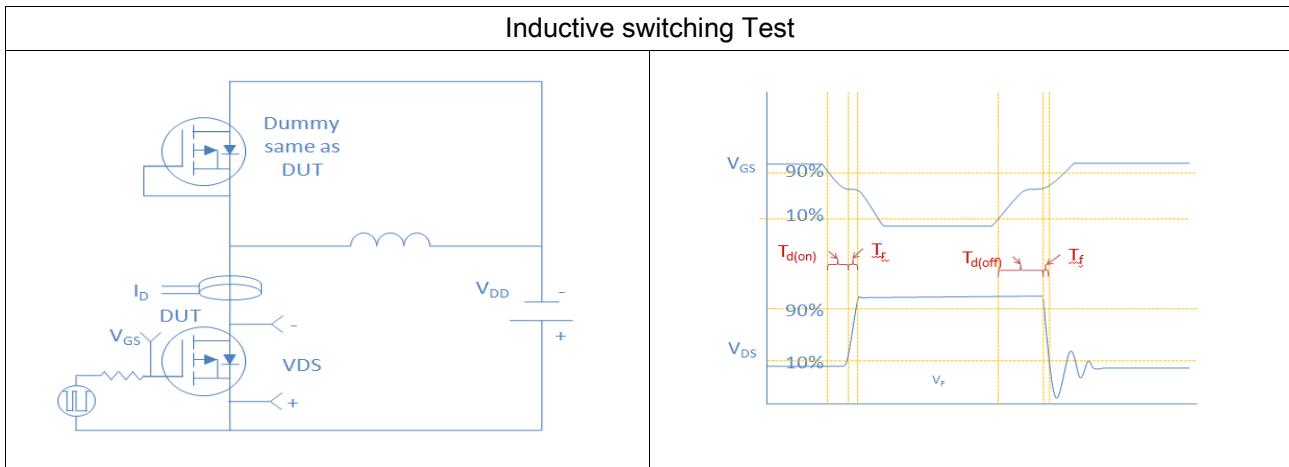


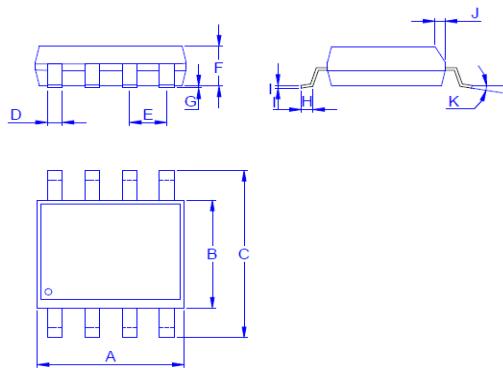
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





Package Outline

SOIC-8, 8leads



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°